WHAT IS CLAIMED IS:

1. A method for handling system management interrupts in a multiprocessor computer system, comprising the steps of:

writing a predetermined signature to a predetermined register of the first processor;

executing in a first processor a command of a software application to cause the first processor to initiate a system management interrupt;

receiving at each processor an instruction that a software system management interrupt has been issued;

entering system management mode at each processor;

saving the register contents of each processor to a memory space associated with each respective processor;

selecting a second processor as the system management interrupt handler;

scanning the contents of the memory space associated with each processor; and

when the second processor locates the saved predetermined signature in one of the memory spaces associated with the processors of the computers system, using the contents of the memory space associated with the predetermined signature for any parameters necessary for the handling of the system management interrupt.

2. The method for issuing and handling system management interrupts in a multiprocessor computer system of claim 1, wherein the step of selecting a second processor as the system management interrupt handler comprises the step of selecting a second processor as the system management interrupt handler according to an arbitration scheme.

3. The method for issuing and handling system management interrupts in a multiprocessor computer system of claim 2, wherein the arbitration scheme is a round robin scheme in which the responsibility for handling the system management interrupt is assigned to each processor in turn.

4. The method for issuing and handling system management interrupts in a multiprocessor computer system of claim 1, wherein the first processor and the second processor are the same processor.

5. The method for issuing and handling system management interrupts in a multiprocessor computer system of claim 1, wherein the step of executing in a first processor a command of a software application to cause the first processor to initiate a system management interrupt comprises the step of executing a software instruction causing to the processor to write to a predetermined port of the chip set of the computer system.

6. The method for issuing and handling system management interrupts in a multiprocessor computer system of claim 5, wherein the predetermined port of the chip set resides in the PCI bridge of the chip set.

7. The method for issuing and handling system management interrupts in a multiprocessor computer system of claim 5, wherein the predetermined port of the chip set resides in the expansion bridge of the chip set.

8. The method for issuing and handling system management interrupts in a multiprocessor computer system of claim 7, further comprising the step of issuing from the expansion bridge an instruction causing each of the processors of the system to enter system management mode.

9. A computer system, comprising:

a first processor;

a second processor;

a chip set, the chip set including a bus bridge coupling a first bus of a first format to a second bus of a second format;

a memory having a memory space reserved for each processor of the computer system, the reserved memory space being used for the storage of the contents of the register of each processor in the event that a processor of the computer system enters system management mode; and

wherein each of the processors is capable of issuing an instruction causing the issuance of a system management interrupt and thereby causing each of the processors to receive from the chip set a system management interrupt, and, in the case of the processor selected for the handling of the interrupt, scanning the memory space to locate a signature issued by the processor initiating the software system management interrupt to permit the selected processor to locate the parameters passed by the processor that issued the instruction that caused the issuance of the system management interrupt.

10. The computer system of claim 9, wherein the instruction issued by the processor is a write instruction.

11. The computer system of claim 10,

wherein the write instruction is received by the chip set of the computer system; and

wherein the chip set of the computer system issues the instruction that causes the processors of the system to enter system management mode.

12. The computer system of claim 11, wherein the write instruction is received at the PCI bridge of the chip set.

13. The computer system of claim 11, wherein the write instruction is received at the expansion bus bridge of the chip set.

14. The computer system of claim 9, wherein each processor includes a predetermined register for receiving a data signature indicating that the processor of the register caused the issuance of a software system management interrupt.

15. The computer system of claim 14, wherein the data signature is saved to the memory space reserved for the processor of the register and identifies the processor that issued the instruction that caused the issuance of the system management interrupt.

16. A method for handling system management interrupts in a multiprocessor computer system in which less than all of the processors of the computer system have been designated for the handling of software system management interrupts, comprising the steps of:

issuing an instruction from a first processor of the system to a chip set of the computer system;

receiving the instruction at the chip set of the computer system and, in response, issuing a command causing the processors of the system to enter system management mode;

writing a software system management interrupt signature to a predetermined register of the first processor as an indication that the first processor issued the command that caused the processors of the system to enter system management mode;

writing the content of the registers of each processor to a memory location, the memory location including a memory space reserved for and associated with the register contents of each processor;

transmitting a software system management interrupt to a second processor of the computer system, the second processor including a system management interrupt handler, and the second processor locating, in response, to the receipt of the software system management interrupt the software system management interrupt signature in the memory location; and

retrieving for use by the system management interrupt handler as parameters register contents saved by the first processor to the memory space associated with the software system management interrupt.

17. The method for handling system management interrupts in a multiprocessor computer system of claim 16 wherein the first processor does not include a system management interrupt handler.

18. The method for handling system management interrupts in a multiprocessor computer system of claim 16 wherein only the second processor includes a system management interrupt handler.

19. The method for handling system management interrupts in a multiprocessor computer system of claim 16 wherein the instruction from the first processor to the chip set of the computer system is a write command to a predetermined port of the chip set.

20. The method for handling system management interrupts in a multiprocessor computer system of claim 19 wherein the write command is received and the software system management interrupt is issued by the PCI bridge of the chip set.

21. The method for handling system management interrupts in a multiprocessor computer system of claim 19 wherein the write command is received and the software system management interrupt is issued by the expansion bus bridge of the chip set.

22. A method for handling system management interrupts in a multiprocessor computer system, comprising the steps of:

receiving at one of the processors of the computer system a system management interrupt;

scanning the memory location containing the saved context of each processor of the computer system;

locating in the memory location a signature identifying the saved context of the processor that issued the instruction that caused the system management interrupt; and

retrieving from the saved context of the processor the parameters necessary for the handling of the system management interrupt.

23. The method for handling system management interrupts in a multiprocessor system of claim 22, wherein the processor that received the system management interrupt is not the same as the processor that issued the instruction that caused the system management interrupt.

24. The method for handling system management interrupts in a multiprocessor system of claim 23, wherein the instruction that caused the system management interrupt is a write instruction to a predetermined port in the chip set of the computer system.

25. The method for handling system management interrupts in a multiprocessor system of claim 24, wherein the write instruction is received at a predetermined port of the PCI bridge of the computer system.

26. The method for handling system management interrupts in a multiprocessor system of claim 25, wherein the write instruction is received at a predetermined port of the expansion bus bridge of the computer system.

27. The method for handling system management interrupts in a multiprocessor system of claim 26,

wherein the processor that receives the system management interrupt includes a system management interrupt handler; and

wherein the processor that issued the instruction that caused the system management interrupt has not been designated for the hanlding of system management interrupts.

handling
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